Core Assignment file Configuration improperly will cause platform CPU overload or dispatch insufficiently and low throughput.

Confirm CPU type of BBU: if D-2177NT or D-2187NT

```
[root@sg-gnb ~]# cat /proc/cpuinfo | grep name | cut -f2 -d: | uniq -c
     28  Intel(R) Xeon(R) D-2177NT CPU @ 1.90GHz
[root@sg-gnb ~]#
```

Need modify below files:

/opt/bbu/oam/cm; CoreAssignment.conf, dataplane_env, protStackCfg.sh

/opt/bbu/phy; 2177CoreAssignment.conf (Depends on the CPU type)

1. Stop protocol stack before make the changes:

#sp.sh -k

2. Modify CoreAssignment.conf

```
{LteCpuInfo->}
CoreNumForLteRt = 8; # number of core for LTE RT thread
# l1d use 1, 25,27
# core id for LTE RT thread
CoreId[0] = 3;
CoreId[1] = 4;
CoreId[2] = 5;
CoreId[3] = 6;
CoreId[4] = 7;
CoreId[5] = 8;
CoreId[6] = 9;
CoreId[7] = 17;
CoreId[8] = 18;
CoreId[9] = 19;
CoreId[10] = 20;
CoreId[11] = 21;
CoreId[12] = 22;
CoreId[13] = 23;
{/LteCpuInfo}

# CPU information for Front end interface
{FeIfCpuInfo->}
CoreNumForIf = 1; # number of core for front end interface
# core id for front end interface
CoreId[0] = 1;
{/FeIfCpuInfo}

# CPU information for hardware control
{HwCtrlCpuInfo->}
CoreNumForHwCtrl = 4; # number of core for LDPC hardware control
# core id for hardware control
CoreId[0] = 2;
CoreId[1] = 2;
CoreId[2] = 2;
CoreId[3] = 2;
{/HwCtrlCpuInfo}
```

3. Modify dataplane_env

```
#  CPU resources
#

# Put available cores here
cpus=(14 12 13 26 27)

#
#CPU core assignment
#

# UP Cores
PDCP_SYS_TIMER_CORE=${cpus[0]}
BH_IO_DISPATCH_CORE=${cpus[1]}
BH_WORKER_CORE="${cpus[2]},${cpus[4]}"
BH_CORE_MASK=0x03000000
BH_WORKER_QDISC=1

export PDCP_SYS_TIMER_CORE BH_IO_DISPATCH_CORE BH_WORKER_CORE BH_CORE_MASK BH_WORKER_QDISC

# OFP_PKT_I/O_Cores
OFP_BH_PKIO_CORE="${cpus[1]},${cpus[2]}"

export OFP_BH_PKIO_CORE

# OFP_APP_Cores
#OFP_APP_CORE=${cpus[0]}"

#export OFP_BH_APP_CORE

# FCH_aysnc
BH_FCH_ASYNC_IO_CORE=${cpus[3]}

export BH_FCH_ASYNC_IO_CORE
```

4. Modify protStackCfg.sh

```
oamprocess_LOG_MAX_NUM=10
odsnameserver_LOG_MAX_NUM=10
callp_LOG_MAX_NUM=10
gnb_LOG_MAX_NUM=10
gtpctrl_LOG_MAX_NUM=10
l2_LOG_MAX_NUM=10
bh_LOG_MAX_NUM=10
pyacs_port=8400
OAM_CPU=14
ODSNAMESERVER_CPU=14
CTRL_CPU_0=24
CTRL_CPU_1=25
CTRL_CPU_2=26
CTRL_CPU_3=27
TTI_CPU_0=10
TTI_CPU_1=11
TTI_CPU_2=12
TTI_CPU_3=13
RLC_RX_THRD_CPU_MAC0=10
RLC_RX_THRD_CPU_MAC1=11
RLC_RX_THRD_CPU_MAC2=12
RLC_RX_THRD_CPU_MAC3=13
RLC_GR_THRD_OFFSET=0
cellNum=1
phyNum=1
cell0_merge_num=1
cell1_merge_num=1
run_phy_flag=true
```

5. Modify 2177CoreAssignment.conf

(Note: No service impaction if not modify file **2177CoreAssignment.conf** , but it will report mismatch alarm with cm file, so suggest to modify at same time)

```
CoreNumForLteRt = 8;  # number of core for LTE RT thread
# 11d use 1, 25,27
# core id for LTE RT thread
CoreId[0] = 3;
CoreId[1] = 4;
CoreId[2] = 5;
CoreId[3] = 6;
CoreId[4] = 7;
CoreId[5] = 8;
CoreId[6] = 9;
CoreId[7] = 17;
CoreId[8] = 18;
CoreId[9] = 19;
CoreId[10] = 20;
CoreId[11] = 21;
CoreId[12] = 22;
CoreId[13] = 23;
{/LteCpuInfo}

# CPU information for Front end interface
{FeIfCpuInfo->}
CoreNumForIf = 1; # number of core for front end interface
# core id for front end interface
CoreId[0] = 1;
{/FeIfCpuInfo}

# CPU information for hardware control
{HwCtrlCpuInfo->}
CoreNumForHwCtrl = 4; # number of core for LDPC hardware control
# core id for hardware control
CoreId[0] = 2;
CoreId[1] = 2;
CoreId[2] = 2;
CoreId[3] = 2;
{/HwCtrlCpuInfo}
```

6. Restart protocol stack after make changes

#restart.tcl